REMARKS

Claims 1-16 are pending in the present application. Claims 4, 10, 11, and 16 were amended to correct typing errors unrelated to the patentability of the claims. No claims are added or canceled. Reconsideration of the claims is respectfully requested.

Amendments were made to the specification to correct errors and to clarify the specification. No new matter has been added by any of the amendments to the specification. The word "digital" was added to the term finite state machine (FSM) in the paragraph on page 2, lines 7 through 20. Support for this change can be found on Page 1, line 27.

Applicants would like to thank the examiner for taking the time to participate in a teleconference on Friday, February 18, 2005. During the call, Applicants and the examiner discussed the examiner's rejection of claims 1, 2, and 15 based on Applicants' Admitted Prior Art. The parties discussed the fact in the Applicants' Admitted Prior Art there was an element designated as FSM 106. Initially, on page 1, line 27 of the Specification, an FSM was defined as a digital finite state machine. However, when discussing Applicants' Admitted Prior Art, FSM was referred to as a finite state machine that receives signals in a digital data stream. The parties agreed to change the paragraph in the Specification discussing the Applicants' Admitted Prior Art so that "finite state machine" would read "digital finite state machine" in order to make the meaning more clear.

I. 35 U.S.C. § 102, Anticipation, Claims 1, 2 and 15

The examiner has rejected claims 1, 2 and 15 under 35 U.S.C. § 102 as being anticipated by Applicants' Admitted Prior Art (Fig. 1). This rejection is respectfully traversed.

As to claims 1, 2 and 15, the Office Action states:

> With respect to claim 1, Applicant Admitted Prior Art (Fig. 1) discloses a semidigital delay locked loop comprising a) a controllable delay element [102] having a clock input and a phase input, and a clock signal output, wherein signals on the clock signal output have a changing phase controlled by phase data received at the phase input; b) a phase detector [104], a first input, a second input, an up output, and a data output, wherein data [DATin] is received at the first input, the second

input is connected to the clock signal output, and wherein the phase detector generates up signals through the up output and down signals through the down output in response to data received at the first input; and c) an analog based finite state machine [106] having an up input connected to the up output, a down input connected to the down output, and phase output connected to the phase input of the controllable delay element, wherein the analog based finite state machine generates the phase data in response to up signals and down signals received from the phase detector.

Office Action dated December 7, 2004, pages 2 and 3.

Independent claim 1 recites:

1. A semidigital delay-locked loop circuit comprising:
a controllable delay element having a clock input and a phase input, and a clock signal output, wherein signals on the clock signal output have a changing phase controlled by phase data received at the phase input;
a phase detector, a first input, a second input, an up output, a down output, and a data output, wherein data is received at the first input, the second input is connected to the clock signal output, and wherein the phase detector generates up signals through the up output and down signals through the down output in response to data received at the first input; and
an analog based finite state machine having an up input connected to the up output, a down input connected to the down output, and phase output connected to the phase input of the controllable delay element, wherein the analog based finite state machine generates the phase data in response to up signals and down signals received from the phase detector.

Independent claim 1 recites the feature of "an analog based finite state machine having an up input connected to the up output, a down input connected to the down output, and phase output connected to the phase input of the controllable delay element, wherein the analog based finite state machine generates the phase data in response to up signals and down signals received from the phase detector." As discussed in the teleconference on Friday, February 18, 2005, Applicants' Admitted Prior Art does not teach this feature. Applicants' Admitted Prior Art, on page 2, lines 7 through 20, shows a digital finite state machine, not an analog based finite state machine, as recited in claim 1. The cited text is as follows:

> Turning to **Figure 1**, a block diagram of a known semidigital DLL-based CDR using a phase rotator is shown. This prior art CDR includes DLL or PLL circuit **100**, phase rotator **102**, phase detector/sampler (PD/S) **104**, and digital finite state machine (FSM) **106**. DLL or PLL circuit **100** receives a clock reference signal, CLK_{ref}. The output of DLL or PLL circuit **100** is input into phase rotator **102**. In turn, phase rotator **102** generates an output clock signal, CLK_{out} at a frequency commensurate with that of CLK_{ref} and with a phase shift controlled by the action of the phase rotator. Phase detector/sampler **104** receives a digital data stream, DAT_{in}, and a clock signal, CLK_{out}, used to generate information about the phase relationship between CLK_{out} and DAT_{in} and to sample DAT_{in}. Phase detector/sampler **104** also generates an output data stream, DAT_{out}. Phase detector/sampler **104** generates up (UP) or down (DN) signals in a digital data stream, which is received by digital finite state machine (FSM) **106**. In turn, digital finite state machine **106** processes this information to produce appropriate control signals which are sent to phase rotator **102**.

Therefore, Applicants' Admitted Prior Art does not teach the claimed feature of "an analog based finite state machine having an up input connected to the up output, a down input connected to the down output, and phase output connected to the phase input of the controllable delay element, wherein the analog based finite state machine generates the phase data in response to up signals and down signals received from the phase detector." Thus, Applicants' Admitted Prior Art does not anticipate claim 1.

Therefore, for the reasons stated above, Applicants submit that independent claim 1 is patentable over Applicants' Admitted Prior Art because Applicants' Admitted Prior Art does not anticipate the present invention.

Claims 2 and 15 are depend from claim 1. As Applicants have already shown claim 1 is patentable over Applicants' Admitted Prior Art, Applicants submit that dependent claims 2 and 15 are also patentable over the Applicants' Admitted Prior Art at least by virtue of depending from an allowable claim.

Therefore, the rejection of claims 1, 2, and 15 under 35 U.S.C. § 102 has been overcome.

II. Objection to Claims, Allowable Subject Matter

The examiner states that claims 3-14 and 16 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form

including all of the limitations of the base claim and any intervening claims. However, all the claims are allowable over Applicants' Admitted Prior Art. Thus, all the claims should be in condition for allowance.

III. Objection to Claims, Minor Informalities

The examiner states that claims 4 and 16 were objected to because of the following informalities:

Claim 4, line 1, change "1" to – 3 –

Claim 16, line 1, change "1" to – 16 –

In response, Applicants have amended claim 4 accordingly. However, it did not make sense to change claim 16, line 1, from "1" to "16," as the claim would then reference itself. Instead, Applicants have amended claim 16 to depend from claim 4. Accordingly, the objections to claims 4 and 16 have been overcome.

IV. Conclusion

It is respectfully urged that the subject application is patentable over the cited reference and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: _____

Respectfully submitted,

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